

Claims

1 *Sub 1* 1. A multichip module comprising:

2 a plurality of chips, each chip comprising  
3 an unpackaged chip having at least one side surface,  
4 an upper surface, a lower surface, and at least one  
5 contact pad at said upper surface;

6 a structural material surrounding the at  
7 least one side surface of each chip of said plurality  
8 of chips and mechanically interconnecting in spaced,  
9 planar relation said plurality of chips, <sup>11</sup> said  
10 structural material having an upper surface  
11 substantially co-planar with an upper surface of each  
12 chip of said plurality of chips to form a first  
13 substantially co-planar surface, said first  
14 substantially co-planar surface comprising a front  
15 surface, and such that a lower surface of said  
16 structural material is substantially parallel with a  
17 lower surface of each chip of said plurality of chips  
18 to form a second surface, said second surface  
19 comprising a back surface; and

20 an in situ processed layer <sup>12</sup> disposed on said  
21 front surface, said in situ processed layer  
22 comprising a material different from said structural  
23 material mechanically interconnecting said plurality  
24 of chips, said in situ processed layer including via  
25 openings to at least some contact pads at the upper  
26 surfaces of said plurality of chips for electrical  
27 connection thereto.

1           2. The multichip module of claim 1, wherein  
2 said structural material has a thickness equal to a  
3 thickest chip of said plurality of chips such that  
4 the upper surface of the structural material is  
5 substantially co-planar with the upper surface of the  
6 thickest chip to form said first substantially co-  
7 planar surface, and such that a lower surface of the  
8 structural material is substantially co-planar with a  
9 lower surface of said thickest chip of said plurality  
10 of chips to form a second substantially co-planar  
11 surface, said second substantially co-planar surface  
12 comprising said back surface.

1           <sup>2</sup>/~~2~~. The multichip module of claim 1, further  
2 comprising an intrachip metallization layer  
3 comprising metallization within each via opening  
4 electrically connected to a corresponding contact pad  
5 of said at least some contact pads, wherein  
6 metallization over each chip is isolated from  
7 metallization over each other chip of said plurality  
8 of chips such that said intrachip metallization layer  
9 fails to electrically interconnect any chips of said  
10 plurality of chips.

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1 ~~Sub 2/4~~ 4. The multichip module of claim 1, wherein  
2 each chip of said plurality of chips has a common  
3 thickness, and wherein said structural material  
4 surrounding and mechanically interconnecting said  
5 chips in spaced planar relation comprises a thickness  
6 equal to said common thickness of said plurality of  
7 chips such that said second surface comprises a  
8 second substantially co-planar surface wherein the  
9 lower surface of said structural material is  
10 substantially co-planar with the lower surface of  
11 each chip of said plurality of chips, and wherein  
12 said first substantially co-planar surface comprising  
13 said front surface is parallel to said second  
14 substantially co-planar surface comprising said back  
15 surface.

1 ~~3~~ 5. The multichip module of claim 1, further  
2 comprising a multi-layer structure disposed over said  
3 in situ processed layer, said multi-layer structure  
4 including a chip interconnect metallization layer  
5 electrically interconnecting at least some chips of  
6 said plurality of chips.

1 ~~Sub 3/7~~ 6. The multichip module of claim 5, wherein  
2 said multi-layer structure further comprises a  
3 release layer disposed over said in situ processed  
4 layer, said release layer being thermally or  
5 chemically removable without removing said in situ  
6 processed layer.

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5. The multichip module of claim ~~4~~, wherein  
said release layer comprises a thermoplastic  
transition layer disposed on said in situ processed  
layer, said release layer being removable with  
application of heat to said thermoplastic transition  
layer.

6. The multichip module of claim ~~5~~, wherein  
said multi-layer structure comprises a first multi-  
layer structure and is disposed over said in situ  
processed layer on said front surface, and said  
multichip module further comprises a second multi-  
layer structure disposed over said back surface.

7. The multichip module of claim ~~6~~, wherein  
said second multi-layer structure comprises a  
preprocessed printed circuit board conductively  
secured to said back surface.

8. The multichip module of claim ~~7~~, further  
comprising at least one conductive through connect  
disposed within said structural material and  
extending between said front surface and said back  
surface for facilitating electrical interconnection  
of said first multi-layer structure and said second  
multi-layer structure.

9. The multichip module of claim ~~8~~, further  
comprising at least one surface mount electronic  
component disposed on an exposed surface of at least  
one of said first multi-layer structure and said  
second multi-layer structure.

<sup>10</sup>  
~~12~~ 12. The multichip module of claim ~~11~~<sup>9</sup>, wherein  
said at least one surface mount electronic component  
comprises a first surface mount electronic component  
disposed on an exposed surface of said first multi-  
layer structure and a second surface mount electronic  
component disposed on an exposed surface of said  
second multi-layer structure, said first surface  
mount electronic component and said second surface  
mount electronic component being electrically coupled  
through said at least one conductive through connect  
in said structural material.

<sup>11</sup>  
~~13~~ 13. The multichip module of claim 1, wherein at  
least one chip of said plurality of chips comprises a  
bare integrated circuit chip.

<sup>12</sup>  
~~14~~ 14. The multichip module of claim 1, wherein  
each chip of said plurality of chips comprises a bare  
integrated circuit chip.

*Sub 15*  
~~15~~ 15. The multichip module of claim 14, wherein  
each chip of said plurality of chips has an equal  
thickness such that the upper surface of each chip is  
co-planar with said front surface and the lower  
surface of each chip is co-planar with said back  
surface, said back surface comprising a planar main  
surface of the multichip module.

<sup>14</sup>  
~~16~~ 16. The multichip module of claim ~~15~~<sup>18</sup>, further  
comprising a heat sink in physical contact with said  
back surface.

<sup>13</sup>  
~~17~~. The multichip module of claim 1, wherein  
1 said in situ processed layer disposed on said front  
2 surface comprises a photo-patternable dielectric  
3 material.  
4

<sup>14</sup>  
~~18~~. The multichip module of claim <sup>13</sup>~~17~~, wherein  
1 said structural material comprises a polymer  
2 consisting of one of epoxy, urethane and polyimide.  
3

1 *§ 1057* 19. An integrated circuit chip module  
2 comprising:

3 an integrated circuit chip comprising a  
4 bare chip having a substrate, active circuitry  
5 associated with said substrate, an upper surface and  
6 a lower surface, said integrated circuit chip further  
7 comprising multiple electrical contact pads at said  
8 upper surface electrically coupled to said active  
9 circuitry, said integrated circuit chip further  
10 having at least one side with a width defined by said  
11 upper surface and said lower surface;

12 a structural material surrounding said at  
13 least one side of said integrated circuit chip, said  
14 structural material having a top surface  
15 substantially co-planar with said upper surface of  
16 said integrated circuit chip to form a first surface,  
17 said first surface comprising a front surface, and  
18 said structural material having a bottom surface  
19 substantially parallel with said lower surface of  
20 said integrated circuit chip to form a second  
21 surface, said second surface comprising a back  
22 surface;

23 an in situ processed layer disposed on said  
24 front surface, said in situ processed layer  
25 comprising a material different from said structural  
26 material surrounding said at least one side of said  
27 integrated circuit chip, said in situ processed layer  
28 including at least one via opening to at least one  
29 contact pad of said multiple electrical contact pads  
30 at the upper surface of said integrated circuit chip;  
31 and

32 a metallization structure comprising  
33 metallization disposed within said at least one via  
34 opening electrically connecting to said at least one  
35 contact pad of said integrated circuit chip.

1 <sup>21</sup>  
2 ~~20~~ 20. The integrated circuit chip module of claim  
3 ~~19~~, wherein said in situ processed layer comprises a  
photo-patternable dielectric material.

1 <sup>22</sup>  
2 ~~21~~ 21. The integrated circuit chip module of claim  
3 ~~20~~, wherein said structural material comprises a  
4 polymer consisting of one of epoxy, urethane and  
polyimide.

1 <sup>23</sup>  
2 ~~22~~ 22. The integrated circuit chip module of claim  
3 ~~21~~, wherein said metallization structure further  
4 comprises at least one input/output (I/O) contact at  
5 an exposed surface of said module, said at least one  
6 I/O contact being electrically coupled to said at  
7 least one contact pad of said integrated circuit  
8 chip, and being disposed at least partially over said  
9 structural material surrounding said at least one  
side of said integrated circuit chip.

1 ~~Stop~~ 23. The integrated circuit chip module of claim  
2 20, wherein said bottom surface is substantially co-  
3 planar with said lower surface of said integrated  
4 circuit chip.

1 24. The integrated circuit chip module of claim  
2 20, wherein said back surface comprises an exposed  
3 planar main surface of said integrated circuit chip  
4 module.



1           25. A method for fabricating a multichip module  
2 comprising the steps of:

3                   (a) providing a plurality of chips, each  
4 chip comprising a bare chip having at least one side,  
5 an upper surface, a lower surface, and a contact pad  
6 at said upper surface;

7                   (b) placing said plurality of chips on an  
8 alignment carrier in spaced relation with the upper  
9 surfaces thereof facing said alignment carrier;

10                   (c) surrounding said plurality of chips  
11 with a structural material such that said at least  
12 one side of each chip is covered by said structural  
13 material, an exposed surface of said structural  
14 material being substantially parallel with the lower  
15 surfaces of said said plurality of chips, thereby  
16 defining a back surface; and

17                   (d) affixing said back surface to a process  
18 carrier, and separating said alignment carrier from  
19 said plurality of chips.

1           26. The method of claim 25, further comprising  
2 forming metallization structures above said plurality  
3 of chips to electrically interconnect said chips.

1           27. The method of claim 25, further comprising  
2 forming by in situ processing a dielectric layer on  
3 the upper surfaces of said plurality of chips and an  
4 upper surface of said structural material  
5 substantially co-planar therewith.

1           28. The method of claim 27, further comprising  
2 patterning and forming vias in said in situ formed  
3 dielectric layer, said vias being disposed to expose  
4 at least some contact pads at the upper surfaces of  
5 the plurality of chips for facilitating electrical  
6 connection thereto.

1           29. The method of claim 26, further comprising  
2 forming metallization structures above said in situ  
3 formed dielectric layer, said metallization  
4 structures comprising metallization within said vias  
5 electrically connected to at least some contact pads  
6 exposed by said vias.

1           30. The method of claim 29, wherein said  
2 forming of said metallization structures comprises  
3 forming intrachip metallization within said vias  
4 electrically connected to at least some contact pads  
5 exposed by said vias, wherein intrachip metallization  
6 over each chip is isolated from intrachip  
7 metallization over each other chip of said plurality  
8 of chips such that said intrachip metallization  
9 structures individually fail to electrically  
10 interconnect any two chips of said plurality of  
11 chips.

1           31. The method of claim 27, wherein said  
2 surrounding step (c) includes surrounding said  
3 plurality of chips with the structural material such  
4 that the at least one side surface and the lower  
5 surface of each chip is covered by the structural  
6 material, and removing structural material from the  
7 exposed surface of the structural material until said  
8 structural material has a thickness equal to at least  
9 one chip of said plurality of chips, the exposed  
10 surface of said structural material being co-planar  
11 with the lower surface of said at least one chip.

1           32. The method of claim 31, wherein said  
2 removing comprises lapping said exposed surface until  
3 said structural material has a thickness equal to  
4 said thickness of said at least one chip of said  
5 plurality of chips.

1           33. The method of claim 32, wherein said  
2 lapping comprises lapping said exposed surface until  
3 the lower surfaces of said plurality of chips and  
4 said exposed surface of said structural material are  
5 co-planar.

1           34. The method of claim 27, wherein said  
2 forming step (e) comprises forming a photo-  
3 patternable dielectric layer on the upper surfaces of  
4 the plurality of chips and the upper surface of the  
5 structural material, said photo-patternable  
6 dielectric layer comprising said in situ formed  
7 dielectric layer.

1           35. The method of claim 34, wherein the  
2 structural material of said surrounding step (c)  
3 comprises a polymer consisting of one of epoxy,  
4 urethane, and polyimide.

1           36. The method of claim 33, wherein said  
2 surrounding step (c) comprises:

3                   (i) applying said polymer until said  
4 at least one side of each chip is covered  
5 by said polymer and said polymer has a  
6 thickness at least equal to a thickness of  
7 a thickest chip of said plurality of chips;

8                   (ii) curing said polymer; and

9                   (iii) lapping said polymer from an  
10 exposed surface at least until said exposed  
11 surface of said polymer and a lower surface  
12 of said thickest chip of said plurality of  
13 chips are co-planar, thereby defining said  
14 back surface.

1           37. The method of claim 27, wherein said  
2 placing step (b) includes securing said plurality of  
3 chips to said alignment carrier via an adhesive  
4 layer.

1           38. The method of claim 37, wherein said  
2 affixing step (d) includes providing a process  
3 carrier adhesive on said process carrier for affixing  
4 said back surface thereto, and applying a catalyst  
5 for said process carrier adhesive on said back  
6 surface such that said back surface is substantially  
7 instantaneously affixed to said process carrier upon  
8 physical contact with said process carrier adhesive.

1           39. The method of claim 27, further comprising  
2 providing a first multi-layer structure over said in  
3 situ formed dielectric layer, said first multi-layer  
4 structure including chip interconnect metallization  
5 electrically interconnecting at least some chips of  
6 said plurality of chips.

1           40. The method of claim 39, further comprising  
2 applying a release layer to said in situ formed  
3 dielectric layer prior to said providing of said  
4 first multi-layer structure, said release layer  
5 facilitating subsequent removal of said first multi-  
6 layer structure.

1           41. The method of claim 39, further comprising  
2 affixing at least one surface mount electronic  
3 component to an exposed surface of said first multi-  
4 layer structure such that said at least one surface  
5 mount electronic component is electrically connected  
6 to at least one chip of said plurality of chips.

1           42. The method of claim 39, further comprising  
2 providing a second multi-layer structure disposed  
3 over said back surface.

1           43. The method of claim 42, wherein said  
2 providing of said second multi-layer structure  
3 comprises providing said second multi-layer structure  
4 as a preprocessed printed circuit board and attaching  
5 said preprocessed printed circuit board to said back  
6 surface.

1           44. The method of claim 42, wherein said  
2 placing step (b) includes placing at least one  
3 conductive through connect die commensurate with  
4 placing of said plurality of chips such that said  
5 structural material of said step (c) surrounds a side  
6 of said at least one electrical through connect die,  
7 and wherein said at least one electrical through  
8 connect die electrically couples said first multi-  
9 layer structure and said second multi-layer  
10 structure.

1           45. The method of claim 44, further comprising  
2 a first surface mount electronic component affixed to  
3 an exposed surface of said first multi-layer  
4 structure and a second surface mount electronic  
5 component affixed to an exposed surface of said  
6 second multi-layer structure, said first surface  
7 mount electronic component and said second surface  
8 mount electronic component each being electrically  
9 coupled to at least one chip of said plurality of  
10 chips.

1           46. The method of claim 27, further comprising  
2 testing said plurality of chips for a defective chip  
3 and if identified, repairing said multichip module by  
4 replacing said defective chip.

1           47. The method of claim 46, wherein said  
2   repairing comprises:

3                   (i) transferring said multichip module  
4                   to an alignment plate by affixing said  
5                   alignment plate to an exposed surface of  
6                   said in situ formed dielectric layer and  
7                   temporarily removing said process carrier  
8                   from said plurality of chips;

9                   (ii) removing a defective chip of said  
10                   plurality of chips;

11                   (iii) replacing the defective chip  
12                   with a preprocessed chip of a same chip  
13                   type as the defective chip; and

14                   (iv) surrounding the preprocessed chip  
15                   with structural material to physically bond  
16                   the preprocessed chip to other chips of the  
17                   plurality of chips in the multichip module.

1           48. The method of claim 47, wherein said  
2   removing of said defective chip comprises  
3   mechanically milling or laser ablating said  
4   structural material and said in situ formed  
5   dielectric layer about said defective chip to  
6   facilitate removal of said defective chip.

1           49. The method of claim 47, wherein said  
2 preprocessed chip has a thickness greater than said  
3 thickness of said structural material in said step  
4 (c) and said repairing further comprises subsequent  
5 to said replacing step (iii), lapping a back surface  
6 of said preprocessed chip to a thickness equal to  
7 said thickness of said structural material  
8 surrounding said plurality of chips in said step (c).

1           50. A method for forming a single chip module  
2 comprising employing said multichip module  
3 fabricating method of claim 29, and subsequent  
4 thereto, separating said plurality of chips in said  
5 multichip module such that a single chip module is  
6 formed for each chip of said plurality of chips.

1           51. A method for repairing the multichip module  
2 of claim 1, said method comprising the steps of:

3                   (i) transferring said multichip module  
4 to an alignment plate by affixing said  
5 alignment plate to an exposed surface of  
6 said in situ processed layer;

7                   (ii) removing a defective chip;

8                   (iii) replacing the defective chip  
9 with a preprocessed chip of a same chip  
10 type as the defective chip; and

11                   (iv) surrounding the preprocessed chip  
12 with structural material to physically bond  
13 the preprocessed chip to other chips of the  
14 plurality of chips in the multichip module.



1           52. The method of claim 51, wherein said  
2 removing of said step (ii) chip comprises  
3 mechanically milling or laser ablating said  
4 structural material and said in situ processed layer  
5 about said defective chip to facilitate removing of  
6 said defective chip.

1           53. The method of claim 51, wherein said  
2 preprocessed chip has a thickness greater than said  
3 thickness of said structural material surrounding  
4 said side surfaces of said plurality of chips, and  
5 wherein said method further comprises lapping a back  
6 surface of said preprocessed chip to a thickness  
7 equal to said thickness of said structural material  
8 surrounding said at least one side surface of each  
9 chip of said plurality of chips.

1           54. A method for repairing the multichip module  
2 of claim 5, said method comprising the steps of:

3                   (i) removing said multi-layer structure  
4 disposed over said in situ processed layer;

5                   (ii) affixing an exposed surface of said in  
6 situ processed layer to an alignment plate;

7                   (iii) removing a defective chip;

8                   (iv) replacing the defective chip with a  
9 preprocessed chip of a same chip type as the  
10 defective chip; and

11                   (v) surrounding the preprocessed chip with  
12 structural material to physically bond the  
13 preprocessed chip to other chips of the plurality of  
14 chips in the multichip module.

1           55. The method of claim 54, wherein said  
2 removing said (iii) comprises mechanically milling or  
3 laser ablating said structural material and said in  
4 situ processed layer about said defective chip to  
5 facilitate said removing of said defective chip.

1 ~~Sub 7~~ 56. A multichip module comprising:

2 a plurality of chips, each chip comprising  
3 an unpackaged chip having at least one side surface,  
4 an upper surface, and a lower surface; and

5 structural material surrounding the at  
6 least one side surface of each chip of said plurality  
7 of chips to mechanically interconnect in spaced  
8 planar relation said plurality of chips, said  
9 structural material having an upper surface co-planar  
10 with the upper surfaces of said plurality of chips,  
11 wherein a co-planar front surface is defined thereby,  
12 and wherein a lower surface of said structural  
13 material is substantially parallel with the lower  
14 surfaces of the plurality of chips, thereby defining  
15 a back surface.

1 ~~28~~ 27. The multichip module of claim ~~56~~ 27, wherein  
2 each chip of said plurality of chips includes at  
3 least one contact pad at the upper surface thereof,  
4 said at least one contact pads being exposed at said  
5 co-planar front surface.

1 ~~Sub 8~~ 58. The multichip module of claim 56, wherein  
2 the lower surface of the structural material is  
3 substantially co-planar with the lower surfaces of  
4 the plurality of chips.

1 ~~30~~ 29. The multichip module of claim ~~58~~ 29, wherein  
2 said back surface is adhesively secured to a heat  
3 sink.

\* \* \* \* \*

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